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PTO-1449 (Modified) 6 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. P043D2C3C	SERIAL NUMBER 09/492,982
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE JANUARY 27, 2000	GROUP ART UNIT 2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	4,330,852	May 18, 1982	Redwine et al.	365	221	
	4,703,418	Oct. 27, 1987	James	364	200	
	4,726,021	Feb. 16, 1988	Horiguchi et al.	371	38	
TNT	4,870,562	Sept. 26, 1989	Kimoto et al.	364	200	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
TNT	S56-82961	July 7, 1981	Japan	—	—	YES	
	S57-14922	Jan. 26, 1982	Japan	—	—	YES	
	Sho 60-80193	May 8, 1983	Japan	—	—	YES	
	Sho 60-55459	Mar. 30, 1985	Japan	—	—	YES	
	S61-72350	April 14, 1986	Japan	—	—	YES	
	S63-142445	June 14, 1988	Japan	—	—	YES	
	B63-46864	Sept. 19, 1988	Japan	—	—	YES	
TNT	S64-29951	Jan. 31, 1989	Japan	—	—	YES	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	Watanabe, T.; "Session XIX: High Density SRAMS"; IEEE International Solid State Circuits Conference pp. 266-267 (1987)
TNT	Ohno, C.; "Self-Timed RAM: STRAM"; Fujitsu Sci. TechJ., 24, 4, pp 293-300 (Dec. 1988)
TNT	"Fast Packet Bus for Microprocessor Systems with Caches", IBM Technical Disclosure Bulletin, pp.279-282 (Jan 1989)
TNT	Gustavson, D. "Scalable Coherent Interface"; Invited Paper, COMPCON Spring '89, San Francisco, CA; IEEE, pp. 536-538 (Feb 27-Mar 3, 1989)
TNT	James, D.; "Scalable I/O Architecture for Busses"; IEEE, pp. 539-544 (April 1989)

EXAMINER TAN T. NGUYEN	DATE CONSIDERED 07/31/00

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
TNT	4,205,373	May 27, 1980	Shah et al.	710	128	
TNT	4,845,670	Jul. 4, 1989	Nishimoto et al.	365	78	
	4,509,142	Apr. 2, 1985	Childers	364	900	
	4,183,095	Jan. 8, 1980	Ward	365	189.02	
TNT	4,685,088	Aug. 4, 1987	Ianucci	365	194	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
TNT	0 246 767	April 28, 1987	EPO				
TNT	0 334 552	Mar. 16, 1989	EPO				
TNT	0 276 871	Jan. 29, 1988	EPO				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TNT	European Search Report for EPO Patent Application No. 00 101 1832
TNT	European Search Report for EPO Patent Application No. 89 30 2613
TNT	Z. Amitai, "New System Architectures for DRAM Control and Error Correction", Monolithic Memories Inc., Electro/87 and Mini/Mico Northeast: Focusing on the OEM Conference Record, pp. 1132, 4/31-3, (April 1987)
TNT	N. Siddique, "100-MHz DRAM Controller Sparks Multiprocessor Designs", Electronic Design, pp. 138-141, (Sept 1986)
TNT	H. Kuriyama et al., "A 4-Mbit CMOS SRAM WITH 8-NS SERIAL ACCESS TIME" , IEEE Symposium On VLSI Circuits Digest Of Technical Papers, pp. 51-52, (June 1990)
TNT	J. Chun et al., "A 1.2ns GaAs 4K Read Only Memory", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 83-86, (Nov. 1988)
TNT	A. Fielder et al., "A 3 NS 1K X 4 STATIC SELF-TIMED GaAs RAM", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 67-70, (Nov. 1988)
TNT	JEDEC Standard No. 21C

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